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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/044,178	01/10/2002	Todd Edgar	MIO 0011 N2	3193

7590 02/14/2006

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EXAMINER	
LE, THAO X	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 02/14/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/044,178	EDGAR, TODD
	Examiner	Art Unit
	Thao X. Le	2814

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 February 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. Applicant's request for reconsideration of the finality of the rejection of the last Office action is persuasive and, therefore, the finality of the Office Action dated 01/12/06 is withdrawn. However, the following final Office Action is based on the Applicant's amendment filed on 19 Dec. 2005.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 1-5 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 1-5 rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01. The omitted structural cooperative relationships are: The stop region (14) is a doped semiconductor structure (15B). Recited 'patterning stop region disposed over and in contact with said substrate'

in claim 1-4 omitted the patterned doped semiconductor structure in forming a stop region. Thus, it would make the claim being indefinite.

For the purpose of examination, assuming the claim would read as 'patterning the doped semiconductor structure forming a stop region disposed over and in contact said substrate' for claim 1-2 and 'patterning the doped semiconductor structure forming a stop region including:' for claim 3-4.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 5576240 to Radosevich et al. in view of US 5028990 to Kotaki et al. and US 4888820 to Chen et al.

Regarding claims 1-2, Radosevich discloses a storage container structure in fig. 1 comprising: a layer substrate 11/18, column 2 line 61, including a doped semiconductor structure 12, col. 3 line 35; a single insulating material 13, col. 3 line 25, disposed over and in contact with said substrate, the insulating material

13 of sufficient depth to include a container region (where 14 is located) disposed therein, said container region defining a container cross section having container side walls, a container bottom wall, and a container interior bounded in part by said container side walls and said container bottom wall; patterning said doped semiconductor structure 12 forming a stop region 12 disposed over and in contact with said substrate 11/18 such that a substantially entirely of the width of said container region is defined by an upper surface of said patterning stop region 12, fig. 1; a charge storage lamina 14/15/17 formed over an interior surface of said container region; said charge storage lamina comprising a first conductive film 14, col. 2 line 63, a second conductive film 17, col. 2 line 58, defining a first surface thereon, and an insulating film 15, col. 3 line 7, disposed intermediate said first and second conductive films 14/17; a contact region (outer surface of 17) defined by said charge storage lamina, wherein said contact region defines a contact region cross section having contact region side walls and a contact region bottom wall, and wherein said contact region side walls and said contact region bottom wall are defined by said first surface of said second conductive film 17.

But Radosevich does not disclose an electrical contact in contact with said first surface of said second conductive film such that said electrical contact and said charge storage lamina occupy collectively at least a portion of said container region.

However, Kotaki discloses a storage container structure comprises an electrical contact 16, fig. 10 col. 4 line 68, in contact with said first surface of said second conductive film 14, col. 3 line31, such that said electrical contact and said charge storage lamina occupy collectively at least a portion of said container region. At the time the invention was made; it would have been obvious to one of ordinary skill in the art to use the electrical contact teaching of Kotaki with Radosevich's device, because it would have established an electrical contact with the top plate electrode.

With respect to single substrate, Chen discloses in fig. 2, 5, and 6 a capacitor comprises a patterned stop region 4, wherein the stop region 6 disposed over and in contact with the single substrate 2 in fig. 2, a capacitor comprises a stop region 20 formed on a dielectric layer 22, wherein the dielectric layer disposed over and in contact with the substrate 2 in fig. 5, or a trench capacitor comprises a stop region 4 in the trench and disposed over and in contact with the substrate 2. At the time the invention was made; it would have been obvious to one of ordinary skill in the art to use the various capacitor configuration teaching of Chen with Radosevich's device, because such capacitor configuration is typical in the art, see also fig. 2g and 3g of Madan (US5604659).

Regarding claim 3, Radosevich discloses a storage container structure comprising: a single substrate 11 including a doped semiconductor structure 12,

said substrate including a generally planar upper surface; a single insulating material 13 disposed over and in contact with said generally planar upper surface of said substrate 11, said insulating material including a container region disposed therein (where 14 is located), said container region defining a container cross section having container side walls, a container bottom wall, and a container interior bounded in part by container side walls and said container bottom wall; patterning said doped semiconductor structure forming a stop region 12 including: a lower surface disposed over and in contact with said generally planar upper surface of substrate 11; and an upper surface configured such that the lowermost extension of container bottom wall does not project substantially below upper surface of said patterning stop region 12; a charge storage lamina 14/15/17 over an interior surface of said container region; said charge storage lamina comprising a first conductive film 14, a second conductive film 17 defining a first surface thereon, and an insulating film 15 disposed intermediate said first and second conductive films 14/17; a contact region (top surface of 17) defined by said charge storage lamina, wherein contact region defines a contact region cross section having contact region side walls and a contact region bottom wall, and wherein contact region side walls and contact region bottom wall are defined by a first surface of charge storage lamina.

But Radosevich does not disclose an electrical contact in contact with said first surface of said second conductive film such that said

electrical contact and said charge storage lamina occupy collectively at least a portion of said container region.

However, Kotaki discloses a storage container structure comprises an electrical contact 16, fig. 10 col. 4 line 68, in contact with said first surface of said second conductive film 14, col. 3 line31, such that said electrical contact and said charge storage lamina occupy collectively at least a portion of said container region. At the time the invention was made; it would have been obvious to one of ordinary skill in the art to use the electrical contact teaching of Kotaki, because it would have established an electrical contact with the top plate electrode.

With respect to single substrate, Chen discloses in fig. 2, 5, and 6 a capacitor comprises a patterned stop region 4, wherein the stop region 6 disposed over and in contact with the single substrate 2 in fig. 2, a capacitor comprises a stop region 20 formed on a dielectric layer 22, wherein the dielectric layer disposed over and in contact with the substrate 2 in fig. 5, or a trench capacitor comprises a stop region 4 in the trench and disposed over and in contact with the substrate 2. At the time the invention was made; it would have been obvious to one of ordinary skill in the art to use the various capacitor configuration teaching of Chen with Radosevich's device, because such capacitor configuration is typical in the art, see also fig. 2g and 3g of Madan (US5604659).

Regarding claims 4-5, Radosevich discloses a storage container structure comprising: a single substrate 11 including a doped semiconductor structure 12, substrate 11 including a generally planar upper surface, an insulating material 13 disposed over and in contact with said generally planar upper surface of substrate, insulating material 13 including a container region disposed therein (where 14 is located), container region defining a container cross section having container side walls, a container bottom wall, and a container interior bounded in part by container side walls and said container bottom wall; patterning said doped semiconductor structure 12 to form a stop region 12 including: a lower surface in contact with said generally planar upper surface of said substrate 11, and an upper surface configured to define a substantially entirely of said container cross section; a charge storage lamina 14/15/17 over an interior surface of said container region; said charge storage lamina comprising a first conductive film 14, a second conductive film 17, defining a first surface thereon, and an insulating film 15, disposed intermediate said first and second conductive films 14/17; a contact region (top surface of 17) defined by charge storage lamina, wherein contact region defines a contact region cross section having contact region side walls and a contact region bottom wall, and wherein contact region side walls and contact region bottom wall are defined by a first surface of charge storage lamina.

But Radosevich does not disclose an electrical contact in contact with said first surface of said second conductive film such that said electrical contact and said charge storage lamina occupy collectively at least a portion of said container region.

However, Kotaki discloses a storage container structure comprises an electrical contact 16, fig. 10 col. 4 line 68, in contact with said first surface of said second conductive film 14, col. 3 line31, such that said electrical contact and said charge storage lamina occupy collectively at least a portion of said container region. At the time the invention was made; it would have been obvious to one of ordinary skill in the art to use the electrical contact teaching of Kotaki, because it would have established an electrical contact with the top plate electrode.

With respect to single substrate, Chen discloses in fig. 2, 5, and 6 a capacitor comprises a patterned stop region 4, wherein the stop region 6 disposed over and in contact with the single substrate 2 in fig. 2, a capacitor comprises a stop region 20 formed on a dielectric layer 22, wherein the dielectric layer 22 disposed over and in contact with the substrate 2 in fig. 5, or a trench capacitor comprises a stop region 4 in the trench and disposed over and in contact with the substrate 2. At the time the invention was made; it would have been obvious to one of ordinary skill in the art to use the various capacitor configuration teaching of Chen with

Radosevich's device, because such capacitor configuration is typical in the art, see also fig. 2g and 3g of Madan (US5604659).

Response to Arguments

6. Applicant's arguments with respect to claims 1-5 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thao X. Le whose telephone number is (571) 272-1708. The examiner can normally be reached on M-F from 8:00 AM - 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael M. Fahmy can be reached on (571) 272 -1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Thao X. Le
08 Feb. 2006